# DEVELOPMENT OF A NEURAL ADC-SAR ARCHITECTURE FOR BIOMEDICAL APPLICATIONS

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***ABSTRACT***

*Skin lesions due to neglected tropical skin diseases which are endemic in landlocked areas with a high morbidity rate as very often disabling when not quickly detected and treated like Buruli, ulcer, yawl, leprosy etc. then we need. The development of an electronic diagnostic tool with low power consumption will be of great importance for its landlocked regions without electricity. The main advantage of the SAR ADC is the possibility to avoid power consuming operational amplifiers (OPAMPs), which can therefore be used in these diagnostic devices. In this paper we propose a neural ADC-SAR capable of detecting low power and low voltage signals and capable of converting these analogue signals to digital signals for less power consuming diagnostic devices that can be used in remote areas where these diseases are prevalent. The comparison is made with conventional ADC SAR with an ideal DAC. An electronic neuron DAC is designed from an artificial neural network that learns a sinusoidal signal for testing purposes. The results of the neural module show a regression coefficient very close to 1 (0.99) and an MSE of 0.98 permit us to obtain the best weight of our electronic DAC Neurons. Compared to the ADC-SAR with an ideal DAC our architecture seems to have very good properties regarding signal to noise ratio, ENOB, THD, SFDR and SINAD with low voltage signal (0.5 to 1V). which proves that there is an improvement in the error of non-linearity with our model and it can be implement in biomedical signal which are low power signal.*

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***KEYWORDS***

*Neural DAC, ADC-SAR, Artificial Neural Network, Electronic Neuron.*

## 1. INTRODUCTION

More than 1.000 million people in tropical and subtropical countries are affected by neglected tropical skin diseases, which cost developed countries billions of dollars per year [1]. These neglected tropical diseases (NTDs) persist in very remote localities, usually without electric power. However, early diagnosis of these disabling diseases is a guarantee of therapeutic success to avoid irreversible consequences. This diagnosis requires the acquisition, processing, and analysis of certain complex analog signals (EMG, bioimpedance, etc.). However, in biomedical equipment, the ADC is the most power-hungry electronic circuit. Thus, designing a high-performance ADC that consumes very little electrical energy becomes an imperative for energy autonomous biomedical equipment that can be used in these remote areas for the early diagnosis of these diseases in order to promote rapid management. In the literature, ADC-SARs have been shown to be ideal candidates for such applications [2]. The complexity of these analog signals, for us calls for the development of a kind intelligent and specialized ADC using the optimization properties of artificial neural networks to reduce the non-linearity error that is often due to the ADC-SAR's conventional DAC.

An ADC is a unit or process that transforms analog signals into digital signals at its input. At the ADC's input, a voltage or current signal representing each of these signals is normally present. The continuous time and value analog signal at the input is translated into digital streams that reflect resampled value of the target signal at particular points in time. The main advantage of ADC-SAR is the ability to avoid energy-intensive operational amplifiers, thus requiring less power consumption characteristic. It differs from other converter architectures in that it has medium resolution, medium conversion rate, low power dissipation, good accuracy, and low area requirements. This converter topology is more attractive in biomedical applications and portable devices.

Even if there are several variants of the successive approximation converter, the basic principle is the same: a sequencer (generally called SAR for Successive Approximation Registers), coupled to a digital-to-analog converter (DAC), produces an analog voltage, which is compared to the signal to be converted. The result of this contrast is iterated starting with the most significant bit (MSB) and ending with the least significant bit (LSB) until the digital word and the input signal are precisely balanced. In this algorithm, the value of the most significant bit of an N-bit register is first set to 1 (i.e., 100, ... 0.00). This gives an analog DAC output value of Vr /2, where Vr is the input reference voltage of the analog- to-digital converter.

VCNA is compared with Vin; if it is lower, the value of the most significant bit is logically correct (Vr /2 is lower than Vin) and remains at "1"; if it is higher, the value of the voltage of the most significant bit is too great and it is reset to "0". The algorithm then moves on to the next bit, which it sets to "1". The comparison is repeated with Vin The whole process is repeated until the algorithm has passed all bits.

The performance metrics of an ADC-SAR are:

- Offset voltage error and gain error which can be encountered in all blocks of the converter. Generally caused by mismatch between components, current related gradient variation, and threshold voltage variation [3].
- The differential nonlinearity error (DNL) is a key parameter in the choice of an ADC. In the literature, it is shown that this error must be less than ± 0.5 LSB to ensure good linearity and no absence of codes at the output of the ADC. A DNL < ± 1 LSB is tolerable [3]. This error is generally created by the DAC because of the mismatch of its resistors with R-2R DACs, the effect of the antiparasitic capacitors for DACs with binary-weighted capacitors, the variation of the threshold voltage and the nonlinearity of the blocking sampler [4].

- The Integral Non-Linearity (INL) error is the integral of the DNL error and therefore, this error deteriorates under the effect of the factors stated for the DNL.
- Apart from these static parameters, other dynamic parameters allow us to better understand its frequency response. Among these we can mention:

- The signal to noise ratio reveals the range of noise in the ADC. Some errors come to deteriorate the good value of this parameter. We can quote the quantization noise introduced by the DAC, the thermal noise introduced by the multiple resistors and capacitors of the usual DACs.

- Another specification that tells us about the non-linearity of the ADC-SAR is the effective number of bits (ENOB). It appears that selecting an adapted DAC for an ADC-SAR is critical in limiting these errors and improving the converter's efficiency. For analog-to-

digital converters, the IEEE has developed terminology and test methods. ENOB is described as follows:

$$\mathrm{ENOB} = 0.5\log_2(\mathrm{SINAD}) - 0.5\log_2(1.5) - \log_2\left(\frac{A}{V}\right). \quad (1)$$

V: Full scale voltage

A: peak-to-peak amplitude of the adjusted sine wave

SINAD: Signal-to-noise and distortion ratio
SINAD is given by the following formula:

$$\mathrm{SINAD} = \frac{P_S}{P_{NAD}}. \quad (2)$$

With Ps: signal power; PNAD: noise and distortion power;

The signal to noise ratio, whose expression in decibels is given by the equation, is an important parameter in the characterization of an ADC:

$$SNR_{dB} \approx 1.76 + 6.02B \ \mathrm{dB}. \quad (3)$$

Noise is a direct contributor to the ADC's SNR degradation. Harmonics are generated by nonlinearity, which reduces the SNR obtained.

In this logic, several works have been identified in the literature to overcome these problems.

The authors concentrated on improving the DAC to effect on the following points in order to enhance the output metrics of the ADC-SAR

- Improvement of the data output rate

- Decrease of the energy dissipation which improves the FOM (Figure of Merit)

- The search for a good DNL and INL

- Improvement of the signal to noise ratio which results in a good ENOB.

Thus, Mortezapour et al. [5] propose a current-mode segmented R-2R DAC with a control circuit with an amplifier at the output of the R-2R to reduce the noise created by the R-2R network. However, this technique adds power consumption through the two PDOs that the authors add to the DAC. In the same direction, a similar architecture is introduced by Fayomi et al [6]. Their ADC-SAR uses CNA R-2R in voltage mode by associating a PDO with its output node in high impedance mode. Aleksandr Gusev et al [7]. Instead of the MSB capacitors of a traditional binary weighted DAC, the mentioned circuit employs an additional low-resolution capacitive DAC. The presence of a second DAC affects the amount of the MSB capacitors. thus, improving energy efficiency and achieving a faster operating speed. The table below summarizes this work.

Table 1. Improvement in ADC-SAR

| Travaux | Mortezapour et al. [5] | Ginsbourg et al. [8] | Agnès A et al. [9] | Yan Zhu et al. [10] | Guan-Ying et al. [11] | Lofti R et al. [12] |
|---|---|---|---|---|---|---|
| Technology | DAC R-2R | Capacitif DAC | Capacitive DAC | Capacitive DAC | Capacitive DAC | Capacitive DAC |
| Improvement | Two current output AOPs | Two parallel capacitive chains | Addition of 2 capabilities to the architecture of Baker[3] | Fragmentation of MSB capacity | Adding a clock doubler circuit | Capacity switching technology |
| Metric | Noice Reduction | Energy Consumption reduction | Reduction of the error related to the matching of capacities | DNL and INL reduction | Linearity error reduction | Energy Consumption reduction |
| Voltage (V) | 1 | 1.2 | 1 | 1.2 | 1.2 | 0.5 et 1 |
| Resolution(bits) | 8 | 5 | 12 | 8 | 10 | 10 |
| ENOB | 7.9 | .... | 11.1 | 7.7 | 8.16 | 9.2 |
| FOM | - | 4.4 | 0.064 | 0.014 | 0.095 | 0.017 |
| DNL(LSB) | 0.47 | 0.26 | <±0.2 | ----- | -1/+1.27 | ---- |
| INL (LSB) | 1.14 | 0.16 | <±0.2 | ----- | -2.8/+2.97 | ---- |
| S/B (dB) | ---- | ----- | 68.6 | ----- | ----- | ---- |
| SFDR(dB) | 62.87 | 36 | ---- | 58 | 64.47 | ---- |
| SNDR(dB) | ---- | 26.1 | ---- | 48 | 50.89 | 57 |
| THD (dB) | -60.52 | -41.5 | ---- | ---- | ---- | -60 |

Along with these advantages of classical ADC-SAR architectures, many drawbacks remain, among others: the difficulty in obtaining the optimum sampling rate in order to match the speed for a reasonable duty cycle at low wattage, the conversion time, and the approximation errors, all of which are primarily due to the DAC's properties. To solve these problems, several authors have proposed solutions incorporating artificial intelligence algorithms. Thus, YUSAKU HIRAI et al. in [3] present an approximation error correction is used in a high-precision biomedical sensor system. To improve resolution, the proposed ADC incorporates a stochastic flash ADC into a successive approximation register This is not practical for our study case. In response to this drawback, Beom Kyu Seo I et al, studied a low resolution and high efficiency neural operator in the analog domain [4]. Thus, they design an 8-bit arithmetic circuit with a digital input and digital output artificial neural network with a computational speed of 33.3 MHz and a computational efficiency of 2.21 TOPS / W.

Wen-Cheng Lai et al. build a 24-bit ADC-SAR that provides excellent quality withing minimizing power dissipation by using an artificial intelligence method as convolutional neural network signal detection [13]. Prior to this last study, Daniel Bankman et al [14] placed an upstream of an ADC- SAR, an intelligent switched capacitor system Capable of performing arithmetic operations (scalar product) as mathematical neural network models. This last solution comes to solve the problem of integration of AI by digital systems such as computers from [15] and [16]. This last study proves the effectiveness of AI in ADC-SAR optimization. Jyotindra R. Shakya et al. [17] after noticing that for any oversampled ADC, there is a range in which each sample will be guaranteed by the input bandwidth. Their results show that while there would be benefit in predicting the range of the signal in the digital domain, which allows for better use of process scaling. This saves a significant amount (70%) of energy during the A-D conversion. These different studies show the considerable contribution that an intelligent ADC-SAR can have in the processing of complex signals by integrating computing systems that can simulate mathematical models. However, some authors in the literature have presented electronic models

of neural networks that can be associated with an electrical circuit to execute intelligent models. Robert Plonsey and Jaakko Malmivuo, in an essay entitled "Bioelectromagnetism" presented in chapter 10 of this document electronic models of neurons [18]. Neuron models can be grouped into many categories based on a number of variables. [19]. From these criteria, electronic models of neurons have emerged. One such model is the LEWIS model [20].

Several other models have been developed by researchers such as Leon Harmon who built a neuron model with a simple circuit. With this model, He conducted research in which he reproduced all of the neuron's signature functions. [22]. The main disadvantage of these models for our architecture is their size if it is necessary to make a neural network from this simple neuron but also their very high supply voltage for biomedical applications as we can see in the figure below.

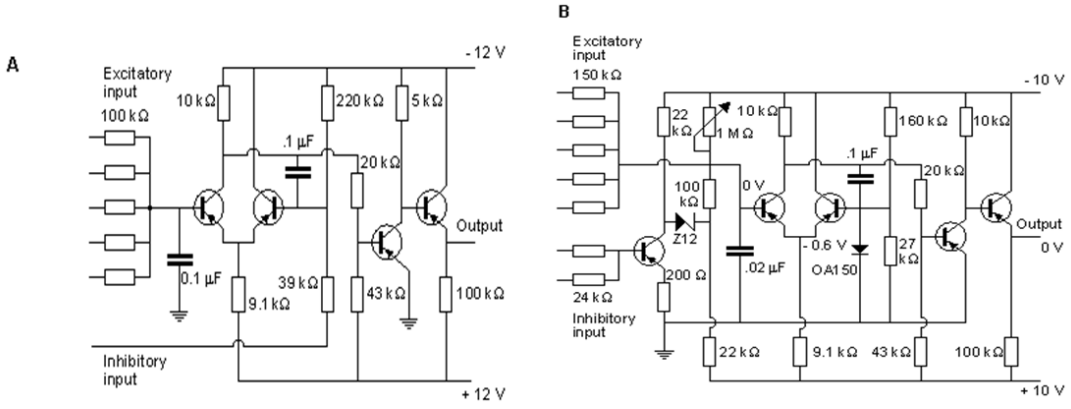


Figure 2. Harmon basic neuron model. (A) and the most advanced version of the circuit (B).

A much more realistic neuron model was developed by Maksim Belyaev et al. [ 23] based on a valium dioxide (VO 2) switch that can implement excitatory and inhibitory coupling. It is a two-layer SNN network consisting of nine input neurons and three output neurons which was modeled for image recognition. The network is capable of recognizing up to 105 frames per second, and the classification process is highly dependent on the temporal parameters of the network and the effect of electrical switching. The network architecture (FIGURE 3) has the potential for further scaling, which increases the speed of recognition and miniaturization of the components [23].

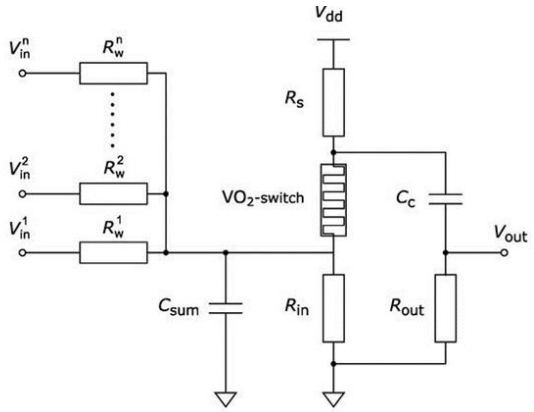


Figure 3. Neuron model of Maksim Belyaev [ 23].

The input and output layers of the Neural Network are connected using synaptic weights, implemented through the resistors Rwi, j, where i is the number of the input neurons and j is the number of the output neuron. The resistance values Rwi, j will change during training.

Based on the above work, we propose a new ADC-SAR model equipped with a neural DAC of the Maksim Belyaev type to contribute to the optimization of the ADC-SAR approximation error.

## 2. METHODOLOGICAL APPROACH OF THE PROPOSED ARCHITECTURE

### 2.1. Presentation of the Architecture of the Neuronal Adc-Sar

The synoptic of the proposed architecture is presented in Figure 4.

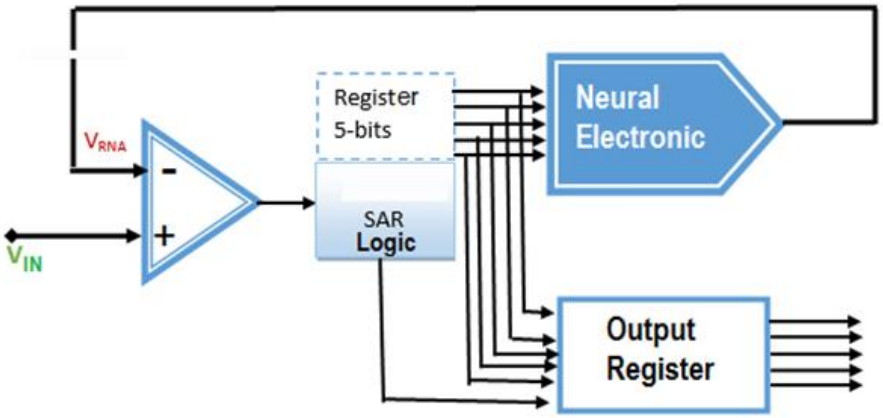


Figure 4. Methodological approach of the ADC SAR NEURONAL architecture

This architecture is that of a conventional ADC-SAR, but the DAC has been replaced by an electronic neuron module which accepts the N-bits from the SAR logic as input and converts them into the corresponding voltage level. This is a reaction to the input stimulus by the neuron which is transformed into an analog voltage level for comparison with the input signal by means of a comparator. It is followed by a SAR logic block which generates a digital signal by successive approximation. The output is a register of N-bits.

#### 2.1.1. Successive Approximation Control Logic

This model uses State flow to model the successive approximation control logic. The state machine serves as a sequencer that first produces a count corresponding to the mid-range, which in this case is 0 volts. The state machine then performs a binary search one-bit position at a time to find the count corresponding to the closest approximation to the input signal sampled in the 5 bits of resolution. The state diagram below shows the operation of the proposed architecture.

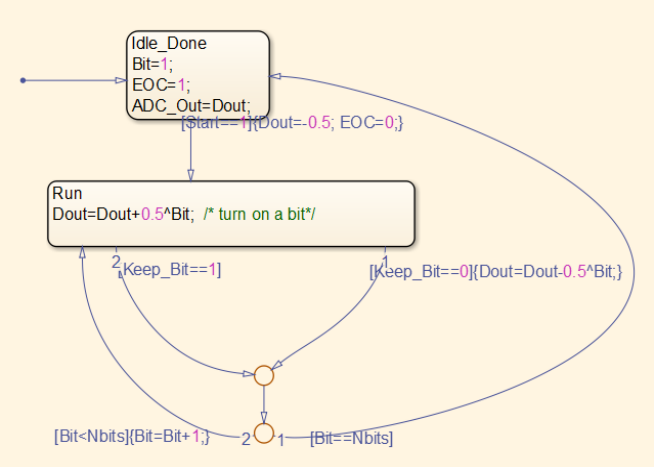


Figure 5. State flow successive approximation

On a particular bit, if the comparator outputs a 1, then that bit is set to 1. Otherwise, that bit position is cleared. Since there are 5 bits, it takes 5 clock cycles for the bit rate clock to complete the conversion for a given input sample.

In this model, the bit rate clock indicated by the block called "ADC Internal Clock" runs at 140 MHz This clock is 14 times faster than the sample rate clock indicated by the block labeled Conversion Clock in the upper left corner of the model. After the control logic goes from bit 4 to bit 0, the end of the conversion line (EOC) goes high, telling the DAC circuit to reset.

### 2.1.2. Implementation of the DAC circuit (electronic neuron)

Our neural network is constituted after learning the results obtained using a DAC from the delta rule algorithm. The input of our neural network is a binary number of five bits and the output is the voltage associated.

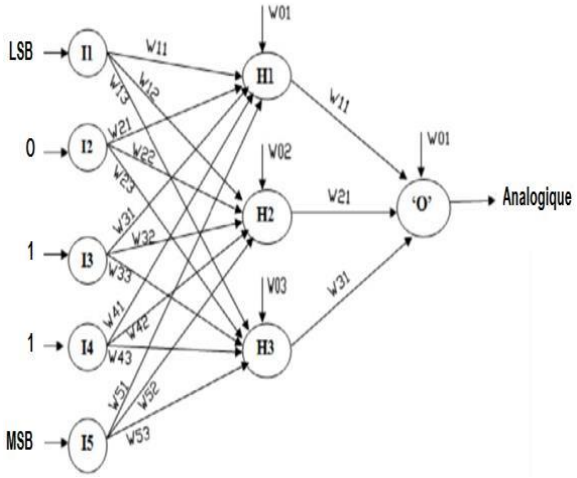


Figure 6. ANN Model

After training our neural network in Matlab as shown in the figure below:

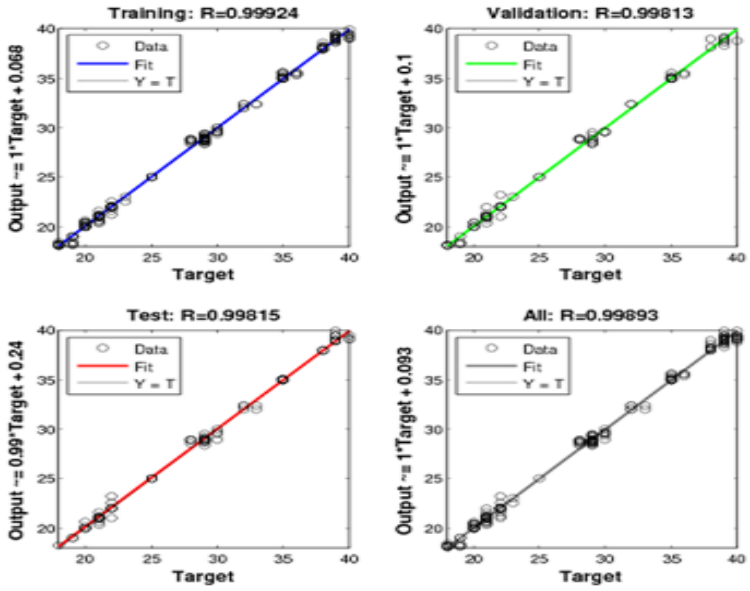


Figure 7. ANN Simulation and validation

We implement this artificial neural network with an electronic circuit presented by the figure below.

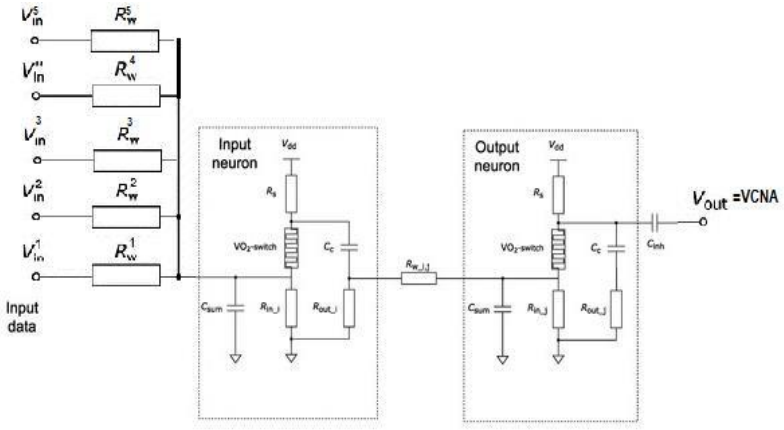


Figure 8. ELECTRONIC structure of the neural network

We use a neural network with a unique hidden layer to find the right Rw weights for our electronic neuron. The learning is supervised from the data from the experiment. The simulation allows us to validate our network because the regression coefficient tends to one as can be seen on the figure below. We initialize the Riw weights in the range from 1.5 kΩ to 2.5 kΩ. After training, we have the values: R1w=1.9kΩ, R2w=1.7 kΩ, R3w=2.1 kΩ, R4w=1.6 kΩ, R5w=2.8 kΩ,

## 2.2. Modelisation of the Neural Adc-Sar

Our ADC-SAR whose Matlab modelisation is presented below is composed of a blocking sampler [15], a comparator, and an approximation register presented in the previous paragraph with its control logic and our designed neural DAC.

The test signal is a sinewave signal. This test signal is sampled at a frequency of 10 MHz the output of the sampler is connected to one input of the comparator. The other is connected to the analog signal output of the neural or ideal DAC. If the output of the sampler is greater than or equal to the output of the DAC, a logical 1 is observed at the output of this comparator. Otherwise it is a logical 0.

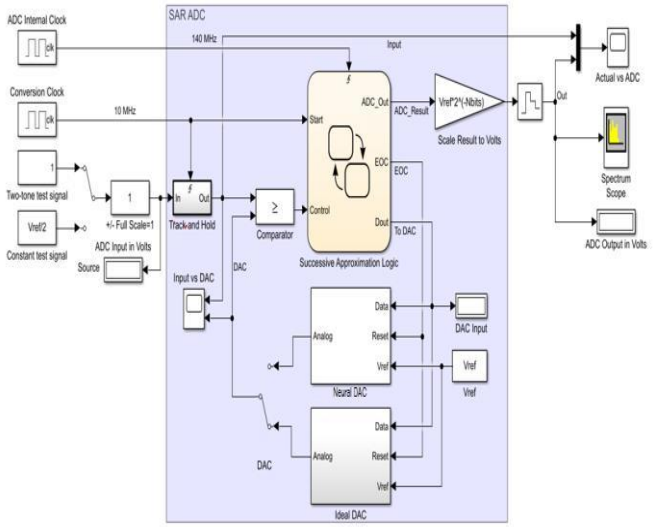


Figure 9. Matlab model of ADC-SAR

## 3. RESULTS AND DISCUSSIONS

### 3.1. Validation of the Neural Module

The model is designed to simulate converters up to 16bits. We equate the voltage output of the ideal DAC in Figure 10 to the neuronal DAC in Figure 8 to test the proposed modeling approach of the ADC., configuring our converter with the following parameters: Nbits = 5;

Fs = 1e7; ADC_clock = Fs*(Nbits+2);

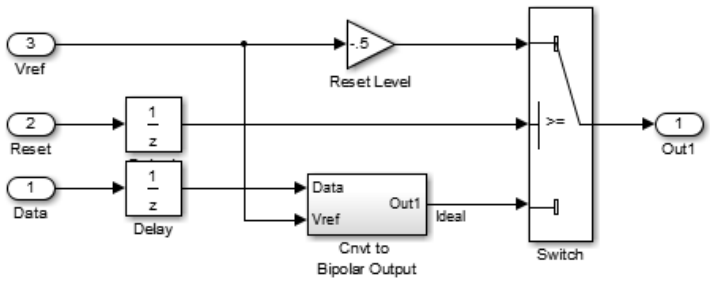


Figure 10. Ideal DAC used for comparison

After simulation of the models under Matlab Simulink, we obtain the results below. For simulation purposes, we use a sinusoidal signal as the analog input signal to the ADC-SAR. The digital equivalent of the signal for the needs of sampling databases are obtained from the OFNUM software. the low voltage signal is chosen (figure below) to approximate biomedical signals

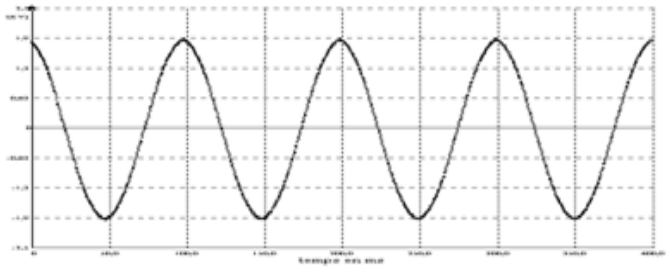

Figure 11. Study signal

We observe on the output signals of the DACs various non-idealities that are similar to distortions in the reconstructed signal. This output is then postprocessed and its frequency response as well as the dynamic performance evaluation are calculated using the Fast Fourier Transform (FFT). This can be seen in figures 12 and 13 below

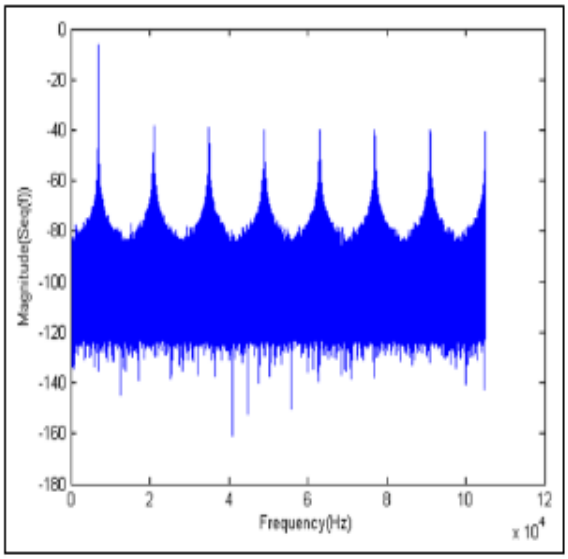


Figure 12. FFT analysis of the ideal DAC output signal

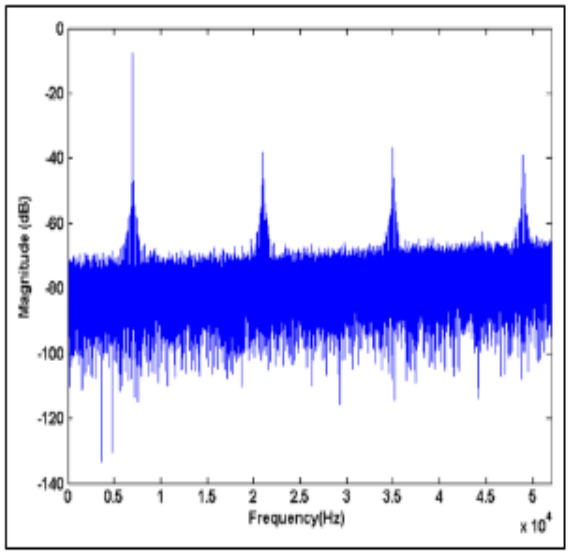


Figure 13. FFT analysis of the neural DAC output signal.

Figures 14, 15, 16 and 17 show a series of simulations of an input signal corresponding to the ADC -SAR with an ideal DAC and the neural DAC under study here. Figure 15 shows a small difference in the ENOB between the two models.

We can notice that both configurations reach their maximum values (4.7 for our model) for a voltage of 1 Volt. Similarly, figure 16 shows the variation of SNR which is about 48 dB for the neural DAC and 49 for the ideal model, which shows an improvement of the ADC-SAR non linearity. Figure 17 shows the variation of THD as a function of the amplitude of the input signal and seems to be the same whatever the amplitude of the signal. We observe that our model as the ideal one has its best performances between 0.5V and 1V.

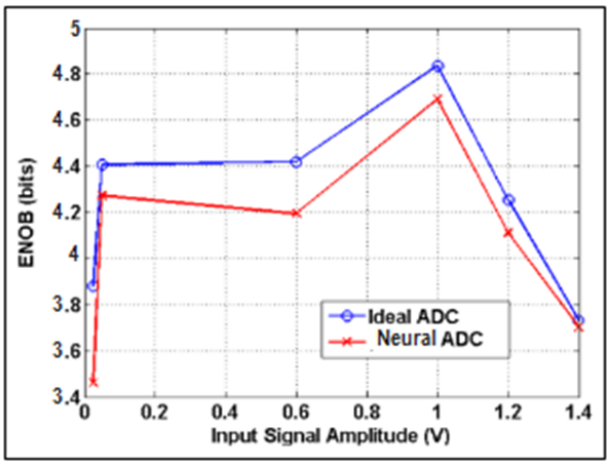


Figure 14. effective number of bits vs. input signal amplitude

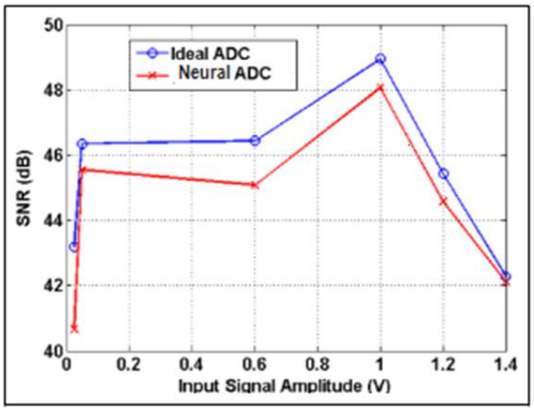


Figure 15. The signal to noise ratio in relation to the input signal

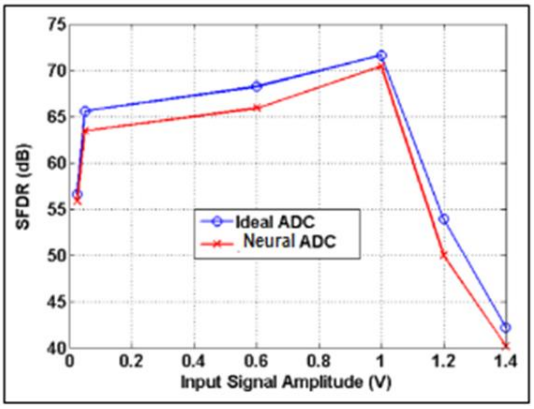


Figure 16. Spurious-free dynamic range in relation to input signal.

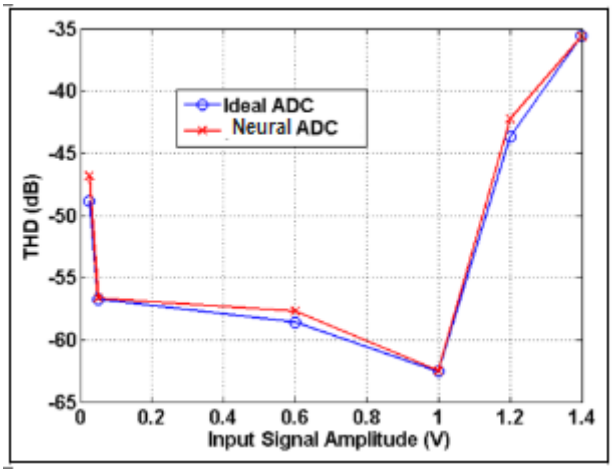


Figure 17. Amplitude of the distortion (THD) in relation to the input signal

The table below provides a comparison with the neural and ideal ADC-SAR designed for the 1V input signal

Table 2. Comparison between Chang's architecture and the proposed one.

| Parameter | Proposed model | ADC SAR with Ideal DAC | Ginsbourg et al. [8] |
|---|---|---|---|
| DAC Model | Neural DAC | Ideal DAC | Two parallel capacitive chains |
| Frequency (sample/ s) | 210 | 210 | 210 |
| Resolution (bits) | 5 | 5 | 5 |
| Input Voltage (V) | 1 | 1 | 1.2 |
| SNR (dB) | 47 | 48 | --- |
| ENOB (bits) | 4,7 | 4,8 | --- |
| SFDR (dB) | 70 | 71 | --- |
| THD (dB) | -62.5 | -62.5 | -41.5 |
| SINAD (dB) | 44,62 | 44,60 | 26.1 |

## 4. CONCLUSIONS

In this study, we propose an architecture of an ADC-SAR integrating, instead of an ideal DAC, an electronic neuron which plays the role of analog to digital converter. The detection of low amplitude signals is generally a challenge in the conversion of biomedical signals, the response properties to small excitations of biological neurons are exploited. The results obtained in comparison to a conventional ADC-SAR seem to be better for sinewave signals. The best result for our model is obtained for input voltages between 0.5 V and 1V. This shows that our model is suitable for small voltages which are characteristic of biomedical signals.

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